IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Currently Amended) A sample and hold circuit having an input and an output, comprising:

at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output;

at least one input switch for selectively connecting said at least one capacitive element to said input;

at least one output switch for selectively connecting said at least one capacitive element to said output; and

an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is substantially limited to said offset voltage, wherein parasitic drain and source diodes (D0, D1) of an NMOS switch are coupled to a voltage that is more negative than an input signal of said NMOS switch in a sample mode, wherein said parasitic drain and source diodes of said NMOS switch are coupled to an output of said amplifier in a hold mode, wherein parasitic drain and source diodes (D2, D3) of a PMOS switch are coupled to a voltage that is more positive than an input signal of said PMOS switch in a sample mode, and wherein said parasitic drain and source diodes of said PMOS switch are coupled to an output of said amplifier in a hold mode.

2. (Original) The sample and hold circuit of claim 1, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

3. (Original) The sample and hold circuit of claim 1, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

4. (Currently Amended) The sample and hold circuit of claim 1, further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in said ~~a~~ hold mode or standard voltages in said sample ~~a write~~ mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

5. (Original) The sample and hold circuit of claim 1, wherein said output provides a DC bias for a magneto-resistive head in a disk drive.

6. (Original) The sample and hold circuit of claim 1, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds.

7. (Original) The sample and hold circuit of claim 1, wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.

8. (Currently Amended) A method for reducing leakage in a sample and hold circuit having at least one capacitive element for retaining a charge, said method comprising the steps of:

configuring at least one input switch to selectively connect said at least one capacitive element to said input;

configuring at least one output switch to selectively connect said at least one capacitive element to said output; ~~and~~

substantially limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element; and

substantially limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a

voltage that is more negative than an input signal of said NMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a hold mode.

9. (Original) The method of claim 8, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

10. (Original) The method of claim 8, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

11. (Currently Amended) The method of claim 8, further comprising the steps of configuring at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in said ~~a~~ hold mode or standard voltages in said sample ~~a write~~ mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

12. (Original) The method of claim 8, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds.

13. (Original) The method of claim 8, wherein said step of limiting a voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.

14. (Currently Amended) A disk drive, comprising:

a magneto-resistive read head; and

a sample and hold circuit having an input and an output, comprising:

(i) at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output;

(ii) at least one input switch for selectively connecting said at least one capacitive element to said input;

(iii) at least one output switch for selectively connecting said at least one capacitive element to said output; and

(iv) an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, wherein parasitic drain and source diodes (D0, D1) of an NMOS switch are coupled to a voltage that is more negative than an input signal of said NMOS switch in a sample mode, wherein said parasitic drain and source diodes of said NMOS switch are coupled to an output of said amplifier in a hold mode, wherein parasitic drain and source diodes (D2, D3) of a PMOS switch are coupled to a voltage that is more positive than an input signal of said PMOS switch in a sample mode, and wherein said parasitic drain and source diodes of said PMOS switch are coupled to an output of said amplifier in a hold mode.

15. (Original) The disk drive of claim 14, wherein said sample and hold circuit is part of a preamplifier for a head bias circuit in a storage system.

16. (Original) The disk drive of claim 14, wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage.

17. (Original) The disk drive of claim 14, further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in

a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches.

18. (Original) The disk drive of claim 14, wherein said output provides a DC bias for a magneto-resistive head in said disk drive.

19. (Original) The disk drive of claim 14, wherein said sample and hold circuit provides a hold time of at least approximately 200 microseconds.

20. (Original) The disk drive of claim 14, wherein said limited voltage drop across at least one of said input and output switches reduces a leakage of said sample and hold circuit.